1. A gate structure with improved endurance characteristics, comprising:

a semiconductor region within a substrate;

source and drain regions contained within said semiconductor region;

at least a gate stack, disposed over said semiconductor region, situated between said source and drain regions and containing a gate insulator layer formed over said semiconductor region, a conductive gate layer disposed over said gate insulator layer, with nitrogen atoms incorporated along the conductive gate layer sidewall.

2. The structure of claim 1 wherein a top gate stack layer is disposed over said conductive gate layer and a sidewall insulator layer, which could be an oxide layer, a nitride layer or a composite layer composed of layers of oxide and nitride, is disposed over sidewalls of said gate stack.

3. The structure of Claim 1 wherein said semiconductor region is a silicon region.

4. The structure of Claim 1 wherein said substrate is a silicon substrate.

5. The structure of Claim 1 wherein said gate insulator layer is an oxide layer.

6. The structure of Claim 1 wherein said conductive gate layer is a polysilicon layer.

7. The structure of Claim 1 wherein said conductive gate layer is a gate of a semiconductor integrated circuit device.

8. The structure of Claim 1 wherein said top gate stack layer is an insulator layer.

9. The structure of Claim 1 wherein said nitrogen atoms extend to the conductive gate layer-gate insulator layer interface in the vicinity of the conductive gate layer edge.

10. A gate structure for flash memory cells with improved endurance characteristics, comprising:

a semiconductor region within a substrate;

source and drain regions contained within said semiconductor region;

at least a gate stack, disposed over said semiconductor region, situated between said source and drain regions and containing a gate insulator layer formed over said semiconductor region, a conductive floating gate layer over said gate insulator layer, an interpoly insulator layer disposed over said conductive gate layer, a conductive control gate layer and a top insulator layer and with a sidewall insulator layer disposed over sidewalls of said gate stack and with nitrogen atoms incorporated along the conductive gate layer sidewall-sidewall insulator layer interface and along the conductive gate layer-gate insulator layer interface in the vicinity of the conductive gate layer edge.

11. The structure of Claim 10 wherein said semiconductor region is a silicon region.

12. The structure of Claim 10 wherein said substrate is a silicon substrate.

13. The structure of Claim 10 wherein said gate insulator layer is an oxide layer.

14. The structure of Claim 10 wherein said conductive floating gate layer is a polysilicon layer.

15. The structure of Claim 10 wherein said floating conductive gate layer is a floating gate of a stacked gate or of a split gate flash memory cell.

16. The structure of Claim 10 wherein said interpoly insulator layer is an ONO layer.

17. The structure of Claim 10 wherein said sidewall insulator layer is an oxide layer, a nitride layer or a composite layer composed of layers of oxide and nitride.

18. The structure of Claim 10 wherein said conductive control gate layer is a polysilicon layer.

19. The structure of Claim 10 wherein said top insulator layer is an oxide layer, a nitride layer or a composite layer composed of layers of oxide and nitride.

20. The structure of Claim 10 wherein a transfer gate stack, comprising: said gate insulator layer; a conductive transfer gate layer, that could be a polysilicon layer, disposed over said gate insulator layer; a top transfer gate insulator layer, that could be an oxide layer or a nitride layer or a combination of these layers, disposed over said transfer gate layer and a transfer gate sidewall insulator layer, that could be an oxide layer or a nitride layer or a combination of these layers; is situated between said gate stack and said source region.

21. A method to fabricate a gate structure with improved endurance characteristics, comprising:

Providing a semiconductor region within a substrate;

Forming source and drain regions contained within said semiconductor region;

Forming at least a gate stack, disposed over said semiconductor region, situated between said source and drain regions and containing a gate insulator layer formed over said semiconductor region, a conductive gate layer disposed over said gate insulator layer and providing a nitrogen-based treatment on the sidewall of said conductive gate layer.

22. The method of Claim 21 wherein said semiconductor region is a silicon region.

23. The method of Claim 21 wherein said substrate is a silicon substrate.

24. The method of Claim 21 wherein said gate insulator layer is an oxide layer.

25. The method of Claim 21 wherein said conductive gate layer is a polysilicon layer.

26. The method of Claim 21 wherein said conductive gate layer is a gate of a semiconductor integrated circuit device.

27. The method of Claim 21 wherein a top gate stack layer, which could be an insulator layer, is formed over said conductive gate layer.

28. The method of Claim 21 wherein a sidewall insulator layer, which could be an oxide layer, a nitride layer or a composite layer composed of layers of oxide and nitride, is formed over sidewalls of said gate stack.

29. The method of Claim 21 wherein said nitrogen-based treatment is either a furnace anneal with NH_3 at a temperature of about 800 degrees Celsius for about 120 minutes or a RTA with NH_3 at a temperature of about 1000 degrees Celsius for about 10 seconds.

30. A method to fabricate a gate structure for flash memory cells with improved endurance characteristics, comprising:

forming a semiconductor region within a substrate;

forming source and drain regions contained within said semiconductor region;

forming at least a gate stack, disposed over said semiconductor region, situated between said source and drain regions and containing a gate insulator layer formed over said semiconductor region, a conductive floating gate layer disposed over said gate insulator layer, an interpoly insulator layer disposed over said conductive gate layer, a conductive control gate layer and a top insulator layer and with a sidewall insulator layer disposed over sidewalls of said gate stack and with a nitrogen treatment performed before forming said sidewall insulator.

31. The method of Claim 30 wherein said semiconductor region is a silicon region.

32. The method of Claim 30 wherein said substrate is a silicon substrate.

33. The method of Claim 30 wherein said gate insulator layer is an oxide layer.

34. The method of Claim 30 wherein said conductive floating gate layer is a polysilicon layer.

35. The method of Claim 30 wherein said conductive floating gate layer is a floating gate of a split gate or of a stacked gate flash memory cell.

36. The method of Claim 30 wherein said interpoly insulator layer is an ONO layer.

37. The method of Claim 30 wherein said sidewall insulator layer is an oxide layer, a nitride layer or a composite layer composed of layers of oxide and nitride.

38. The method of Claim 30 wherein said nitrogen treatment is either a furnace anneal with NH_3 at a temperature of about 800 degrees Celsius for about 120 minutes or a RTA with NH_3 at a temperature of about 1000 degrees Celsius for about 10 seconds.

39. The method of Claim 30 wherein said conductive control gate layer is a polysilicon layer.

40. The method of Claim 30 wherein said top insulator layer is an oxide layer, a nitride layer or a composite layer composed of layers of oxide and nitride.

41. The method of Claim 30 wherein a transfer gate stack, comprising: said gate insulator layer; a conductive transfer gate layer, that could be a polysilicon layer, disposed over said gate insulator layer; a top transfer gate insulator layer, that could be an oxide layer or a nitride layer or a combination of these layers, disposed over said transfer gate layer and a transfer gate sidewall insulator layer, that could be an oxide layer or a nitride layer or a combination of these layers; is situated between said gate stack and said source region.